REMARKS/ARGUMENTS

The Applicants have received the Office action dated September 23, 2004, in which the Examiner: 1) rejected claims 1, 9, 17-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Luiz A. Barroso et al. (U.S. Pat. No. 6,675,265); and 2) rejected claims 1, 9, 17-20 as allegedly anticipated by Laudon (U.S. Pat. No. 5,634,110).

With this Response, Applicants amend claims 1 and 9. Reconsideration is respectfully requested.

I. AMENDMENTS TO THE SPECIFICATION

With this Response, Applicants present a plurality of amendments to the paragraph beginning on page 2, line 9. These amendments merely correct typographical and grammatical oversights. No new matter is presented.

II. DOUBLE PATENTING REJECTIONS

Applicants present concurrently herewith a terminal disclaimer over U.S. Pat. No. 6,675,265, thus obviating the double patenting rejection in the Office action dated September 23, 2004.

III. CLAIM REJECTIONS

A. Claim 1

Claim 1 stands rejected as allegedly anticipated by Laudon. Applicants amend claim 1 to change the claim formatting, to remove the "including" term to ensure that the list is not construed as limiting the number of portions present to just those listed, and to remove the "for" terminology to ensure that 35 U.S.C. § 112, sixth paragraph, is not invoked. These are not narrowing amendments, and the amendments are not made to define over the cited art.

Laudon is directed to cache coherency using flexible directory bit vectors. (Laudon Title). In particular, Laudon is concerned with how to identify nodes in the computer system that need invalidation messages, possibly with fixed size directory entries and as the number of nodes spans from a single partition with a

plurality nodes to several partitions. For example, with respect to the "modified fine bit vector," Laudon states:

> The modified fine bit vector field 704 of the present invention is advantageous because it enables the precise identification of the processing nodes 404 where a memory block 104 is cached, even when more than one processing node 404 caches the memory block 104 (or when more processing nodes 404 than the number of pointers 302 cache the memory block 104 when the binary pointer format in FIG. 3 is used), and even when the number of processing nodes 404 in the computer system 402 is greater than the number of bits in the modified fine bit vector field 704. Thus, the modified fine bit vector field 704 eliminates the transmission of unnecessary invalidation messages (this is a problem that plagued the third conventional solution described above). The present invention achieves this advantage without increasing the size of the directory entries 108.

(Laudon Col 6, line 65 – Col. 13; *see also* Col. 8, lines 21-31;).

In Laudon, each node has a main memory portion 414, and a corresponding directory 106. (Laudon Col. 4, lines 22-33). Further in Laudon, each node (specifically each node's memory controller and network interface) manages its own directory.

> The memory controller and network interface 412 (specifically, the cache coherency mechanism contained therein) in each processing node 404 independently manages each directory entry 108 in the directory 106 contained in the processing node 404.

(Laudon Col. 3, lines 49-53).

Claim 1, by contrast, specifically recites, "input logic that receives a first invalidation request, the invalidation request identifying a memory line of information and a pattern of bits that identify a subset of the plurality of system nodes that potentially store cached copies of the identified memory line... ." Laudon fails to teach (expressly or inherently) or suggest that an "invalidation request" should "identif[y] a memory line of information **and a pattern of bits that identify a subset of the plurality of system nodes that potentially store cached copies of the identified memory line**." For this reason alone claim 1 should be allowed.

Claim 1 further recites, "processing circuitry that **responsive to receipt of the first invalidation request, determines a next node identified by the pattern of bits in the invalidation request and sends to the next node, if any, a second invalidation request corresponding to the first invalidation request**, and that invalidates a cached copy of the identified memory line, if any, in the particular node of the computer system." Laudon fails to teach (expressly or inherently) or suggest that a node that receives an invalidation request should also have processing circuitry that "responsive to receipt of the first invalidation request, determines a next node identified by the pattern of bits in the invalidation request and sends to the next node, if any, a second invalidation request." For this additional reason, Laudon does not teach or fairly suggest the limitations of claim 1.

Based on the foregoing, Applicants respectfully submit that claim 1, and all claims which depend from claim 1 (claims 17 and 18), should be allowed.

B. Claim 9

Claim 9 stands rejected as allegedly anticipated by Laudon. Applicants amend claim 9 to change the claim formatting, to remove the "including" term to ensure that the list is not construed as limiting the number of portions present to just those listed, and to remove the "for" terminology to ensure that 35 U.S.C. § 112, sixth paragraph, is not invoked. These are not narrowing amendments, and the amendments are not made to define over the cited art.

Laudon is directed to cache coherency using flexible directory bit vectors. (Laudon Title). In particular, Laudon is concerned with how to identify nodes in the computer system that need invalidation messages, possibly with fixed size directory entries and as the number of nodes spans from a single partition with a plurality nodes to several partitions. (*See, e.g.*, Laudon Col 6, line 65 – Col. 13; Col. 8, lines 21-31;).

In Laudon, each node has a main memory portion 414, and a corresponding directory 106. (Laudon Col. 4, lines 22-33). Further in Laudon, each node (specifically each node's memory controller and network interface) manages its own directory. (Laudon Col. 3, lines 49-53).

Claim 9, by contrast, specifically recites, "input logic that receives a first invalidation request, the invalidation request identifying a memory line of information and a pattern of bits for identifying a subset of the plurality of system nodes that potentially store cached copies of the identified memory line... ." Laudon fails to teach (expressly or inherently) or suggest that an "invalidation request" should "identif[y] a memory line of information **and a pattern of bits that identify a subset of the plurality of system nodes that potentially store cached copies of the identified memory line.**" For this reason alone claim 9 should be allowed.

Claim 1 further recites, "processing circuitry that, **responsive to receipt of the first invalidation request, determines a next node identified by the pattern of bits in the invalidation request and for sending to the next node, if any, a second invalidation request corresponding to the first invalidation request**, and that invalidates a cached copy of the identified memory line, if any, in the particular node of the computer system." Laudon fails to teach (expressly or inherently) or suggest that a node that receives an invalidation request should also have processing circuitry that "responsive to receipt of the first invalidation request, determines a next node identified by the pattern of bits in the invalidation request and sends to the next node, if any, a second invalidation request." For this additional reason, Laudon does not teach or fairly suggest the limitations of claim 9.

Based on the foregoing, Applicants respectfully submit that claim 9, and all claims which depend from claim 9 (claims 19 and 20), should be allowed.

IV. CONCLUSION

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may

be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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